



Document Version: 3.9
Date: 2006/11/10

Product Functional Specification

12.1 inch Wide XGA Color TFT LCD Module
Model Name: A121EW02 V0

(☒) Preliminary Specification
(☐) Final Specification

Note: This Specification is subject to change without prior notice.



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II Record of Revision

Version and Date	Page	Old description	New Description	Remark
V0. 2006/04/20			First Draft	
V1. 2006/05/19			Spec revised after Mock-up sample finished	
V2 2006/6/16			Review the spec sheet thoroughly.	
	7	None	Absolute Maximum Ratings of the lamp set	3.1
	8	None	Brightness Min.	4.0
	8	None	The condition of the optical measurement	4.0
	13	None	Note1: Define RxINx; Note2: Define RxCLKIN	5.4
	20	None	ESD RA condition	11.0
V3 2006/7/7	7	None	Temperature and Relative Humidity graph	3.0
	7	None	Note 2	3.0
	7	Operating Temperature Max(+70)	Operating Temperature Max: 70	3.0
	7	Storage Temperature Max(+70)	Storage Temperature Max: 70	3.0
	8	Viewing Angle U/D/L/R (50)/(65)/(65)/(65)	Viewing Angle U/D/L/R 50/65/65/65	4.0
	8	None	Luminance Uniformity	4.0
	9	None	Signal Name consistency: DSPTMG→ DE	5.3
	20	Low Temperature Storage: Ta=0℃	Low Temperature Storage: Ta=-20℃	11.0
	20	Low Temperature Operation: Ta=-20℃	Low Temperature Operation: Ta=0℃	11.0
	20	Vibration sweep: 2.9G	Vibration sweep: 3.0G	11.0
	21		Outline Drawing modification	12.0
V3.1 2006/7/12	15	None	Add Lamp(A) and Lamp(B)	5.6
V3.2 2006/7/13	7	+70	Ta:+70/Tp:+71	3.0
	20	Tp: 70	Tp: 71	11.0
	7	None	Ta/Tp definition	3.0
	20	Tp: Panel surface temperature.	Tp: Center point temperature of panel surface.	11.0
V3.3 2006/7/21	6	278.2(W) x 183.7(H) x 13.5(D)	278.2(W) x 183.7(H) x 13.8(D)	2.1
V3.4 2006/7/27	6	278.2(W) x 183.7(H) x 13.5(D)	278.2(W) x 184.0(H) x 13.8(D)	2.1
	6	710g	750g	2.1

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	22	None	Add Note 2	12.0
V3.5 2006/8/18	9		Color / Chromaticity Coordinates (CIE) rang +-0.03	4.0
	22		LVDS 1 st pin marking, redefine inverter cable length;	12.0
V3.6 2006/8/21	9	Bx : 0.09, 0.12, 0.15	Bx: 0.12, 0.15, 0.18	4.0
V3.7 2006/9/15	20	T1/Min: 0.5ms; Max: 10ms	T1/Min: 0.4ms /Max: 50ms	10.0
	20	T7/Max: 10ms	T7/Max: 1000ms	10.0
	23	None	Lot definition	13.0
	24,25	None	Packaging description	14.0
V3.8 2006/10/4	20	T7 min: 0ms; max: 1000ms	Eliminate the definition of T7	10.0
V3.9 2006/11/10	24	Packaging description	Update drawing	14.0

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1.0 Handling Precautions

- 1) Do not press or scratch the surface harder than a HB pencil lead because the polarizers are very fragile and could be easily damaged.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water droplets or oil immediately. Long contact with the droplets may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Protect the module from static electricity and insure proper grounding when handling. Static electricity may cause damage to the CMOS Gate Array IC.
- 7) Do not disassemble the module.
- 8) Do not press the reflector sheet at the back of the module.
- 9) Avoid damaging the TFT module. Do not press the center of the CCFL Reflector when it was taken out from the packing container. Instead, press at the edge of the CCFL Reflector softly.
- 10) Do not rotate or tilt the signal interface connector of the TFT module when you insert or remove other connector into the signal interface connector.
- 11) Do not twist or bend the TFT module when installation of the TFT module into an enclosure (Notebook PC Bezel, for example). It should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside when designing the enclosure. Otherwise the TFT module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local regulations for disposal.
- 13) The LCD module contains a small amount of material that has no flammability grade, so it should be supplied by power complied with requirements of limited power source (2.11, IEC60950 or UL1950).
- 14) The CCFL in the LCD module is supplied with Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



2.0 General Description

This specification applies to the 12.1 inch wide Color TFT/LCD Module A121EW02 V0

This module is designed for a display unit of Portable Video Devices.

The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	307.9(12.1" wide)
Active Area	[mm]	261.12(H) x163.2 (V)
Pixels H x V		1280(x3) x 800
Pixel Pitch	[mm]	0.204 x 0.204
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance(CCFL=6.0mA)	[cd/m ²]	450 Typ.
Contrast Ratio		350:1
Response Time	[msec]	30 Typ.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Weight	[Grams]	750g Typ.
Physical Size	[mm]	278.2(W) x 184.0(H) x 13.8(D)
Electrical Interface		LVDS
Color Depth		262K colors
Temperature Range		
Operating	[°C]	0 to +70
Storage (Shipping)	[°C]	-20 to +70

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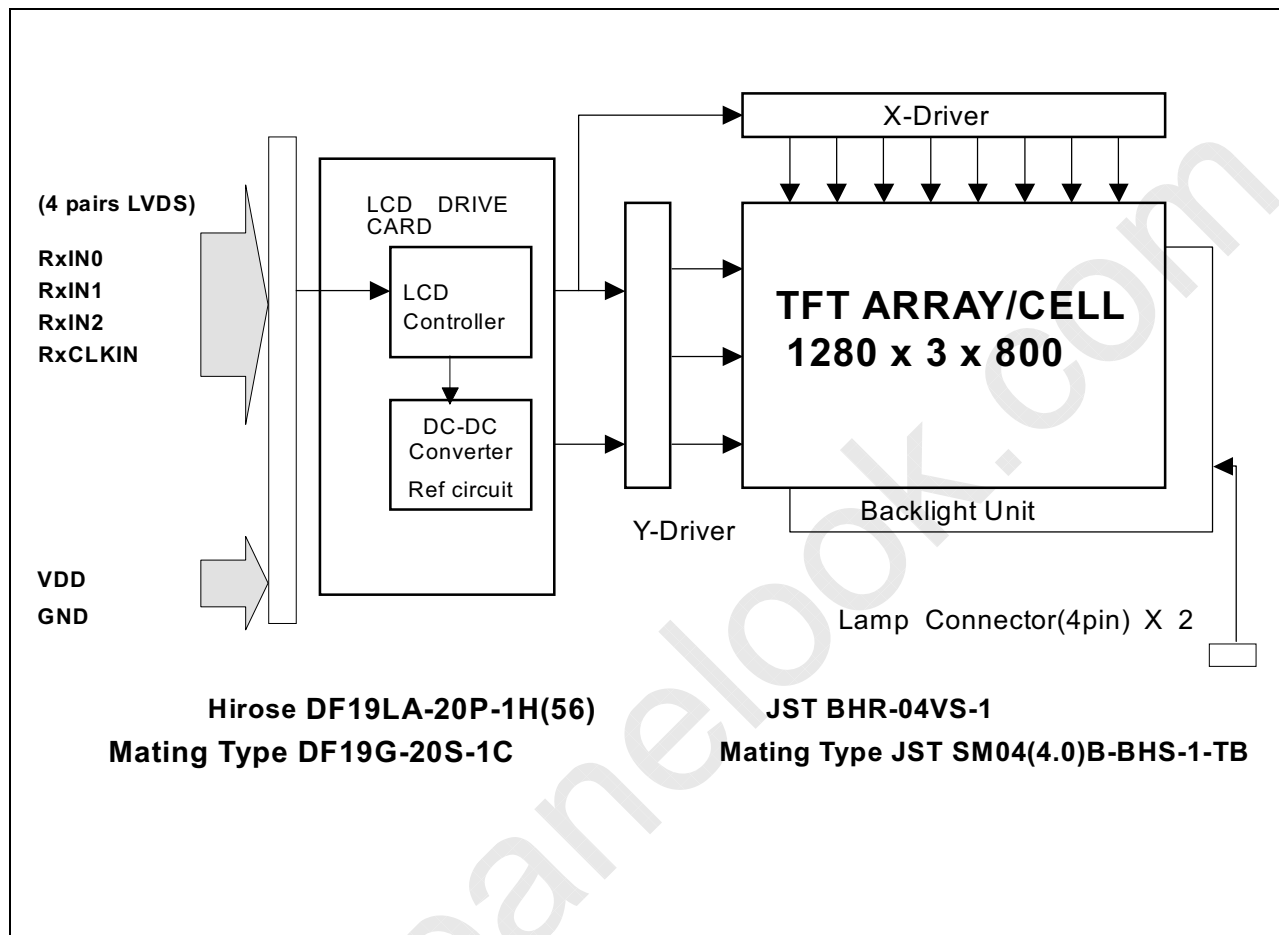
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2.2 Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches Color TFT/LCD Module:



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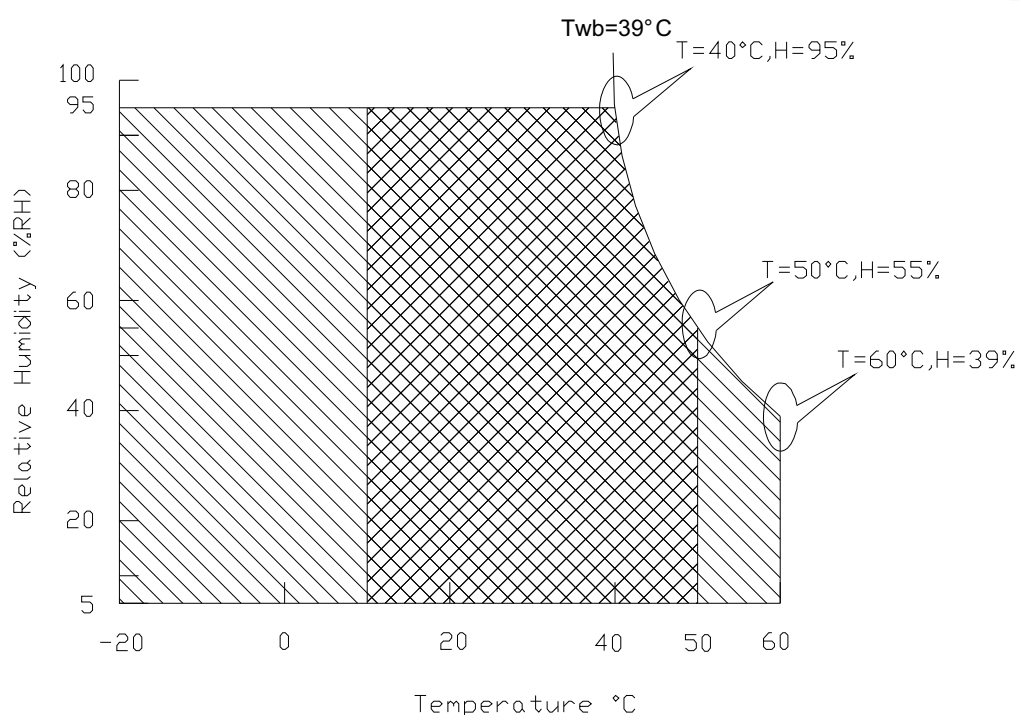
3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
Operating Temperature	TOP	0	Ta:+70/Tp:+71	[°C]	Note 2
Operating Humidity	HOP	5	90	[%RH]	Note 1
Storage Temperature	TST	-20	+70	[°C]	
Storage Humidity	HST	5	90	[%RH]	Note 1

Note 1 : Maximum Wet-Bulb should be 39°C and No condensation.

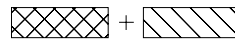
Note2: Ta: Ambient temperature; Tp: Center point temperature of Panel Surface.



Operating Range



Storage Range



Note 2 : High Operating Temperature may cause the slight material variation. We assure under the above condition, the module set keep the function normal display.

3.1 Absolute Maximum Ratings of the lamp set

Item	Symbol	Min	Max	Unit	Conditions
Lamp set current	IL	-	7.0	mArms	Note 1
Lamp set voltage	VL	-	1600	Vrms	Note 2

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Note 1 : Refer to the lamp spec

(a) The above characteristics are measured under the conditions as following:

Ambient temperature: $25 \pm 2^{\circ}\text{C}$; Relative Humidity: $65 \pm 20\%$ RH

(b) The inverter condition in vendor site is: $V_{in}=12\text{V}$, $C=15\text{pf}$, Frequency: 46KHz.

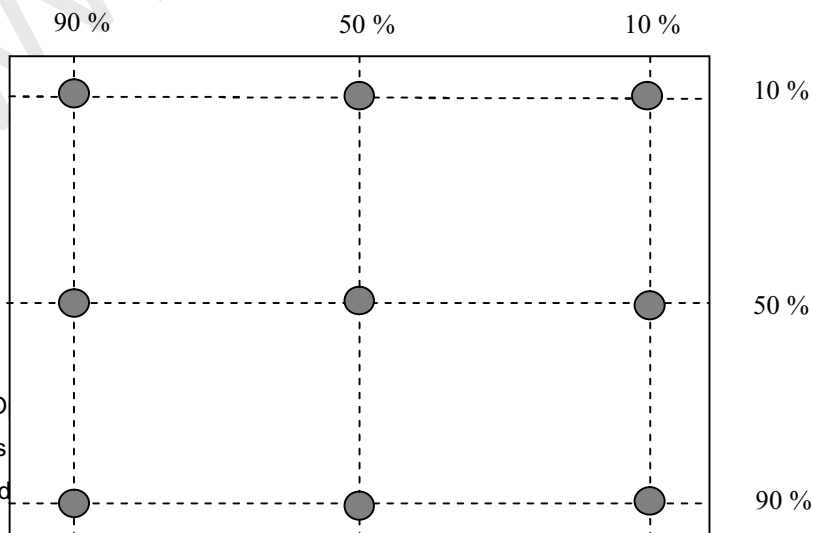
Note 2 : Refer to the connector of the lamp set.

4.0 Optical Characteristics

Item	Unit	Conditions	Min.	Typ.	Max.	Remark
Viewing Angle	[degree]	Horizontal (Right)	50	65	-	
	[degree]	CR = 10 (Left)	50	65	-	
CR: Contrast Ratio	[degree]	Vertical (Upper)	35	50	-	
	[degree]	CR = 10 (Lower)	50	65	-	
Contrast ratio			300	350	-	
Response Time	[msec]	Rising	-	12	50	
	[msec]	Falling	-	18	60	
Color / Chromaticity Coordinates (CIE)		White x	0.28	0.31	0.34	Note1
		White y	0.30	0.33	0.36	Note1
		Red x	0.61	0.64	0.67	
		Red y	0.31	0.34	0.37	
		Green x	0.25	0.28	0.31	
		Green y	0.56	0.59	0.62	
		Bule x	0.12	0.15	0.18	
		Blue y	0.04	0.07	0.10	
White Luminance CCFL @ 6.0mA	[cd/m ²]	Central	400	450	-	Note1
Luminance Uniformity	%		70			Note2

Note 1 : Ambient temperature = 25°C . And lamp current $I_L = 6 \text{ mArms}$. To be measured in the dark room below 10 Lux and to be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 20 minutes operation.

Note 2 : Luminance Uniformity of these 9 points is defined as below:



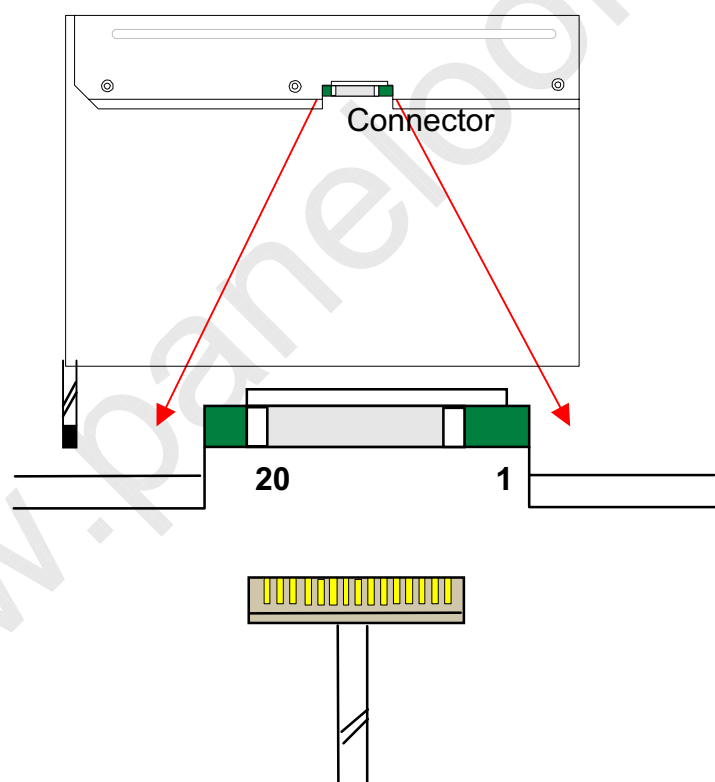
4.1 Signal Description

Signal Name	Description
RxIN0N, RxIN0P	LVDS differential data input (R0~R5, G0)
RxIN1N, RxIN1P	LVDS differential data input (G1~G5, B0~B1)
RxIN2N, RxIN2P	LVDS differential data input (B2~B5, Hsync, Vsync, DE)
RxCLKINN, RxCLKINP	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note1: Start from right side

Note2: Please follow VESA.

Note3: Input signals shall be low or Hi-Z state when VDD is off. Internal circuit of LVDS inputs are as following.



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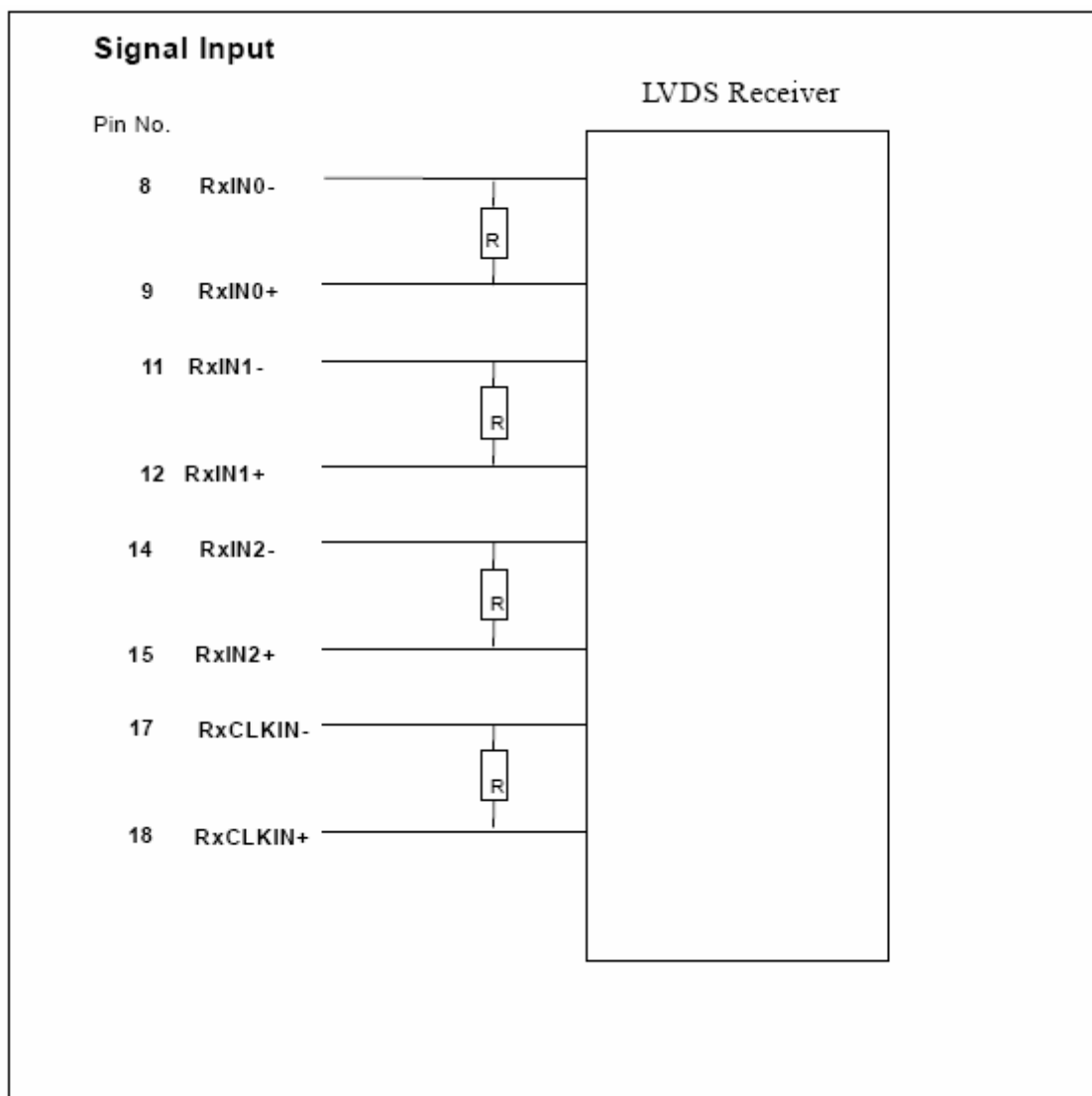
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The module uses a 100ohm resistor between positive and negative data lines of each receiver input



5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	DF19LA-20P-1H(56)
Mating Housing/Part Number	DF19G-20S-1C or compatible

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Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHR-04VS-1
Mating Housing/Part Number	SM04(4.0)B-BHS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VDD _{EDID}
5	AGING	6	CLK _{EDID}
7	DATA _{EDID}	8	RxIN0N
9	RxIN0P	10	GND
11	RxIN1N	12	RxIN1P
13	GND	14	RxIN2N
15	RxIN2P	16	GND
17	RxCLKINN	18	RxCLKINP
19	GND	20	GND

Note: Add 1K ohm resister and connect to grounding as the solution for not adopting Pin4, Pin5, Pin6, and Pin7.

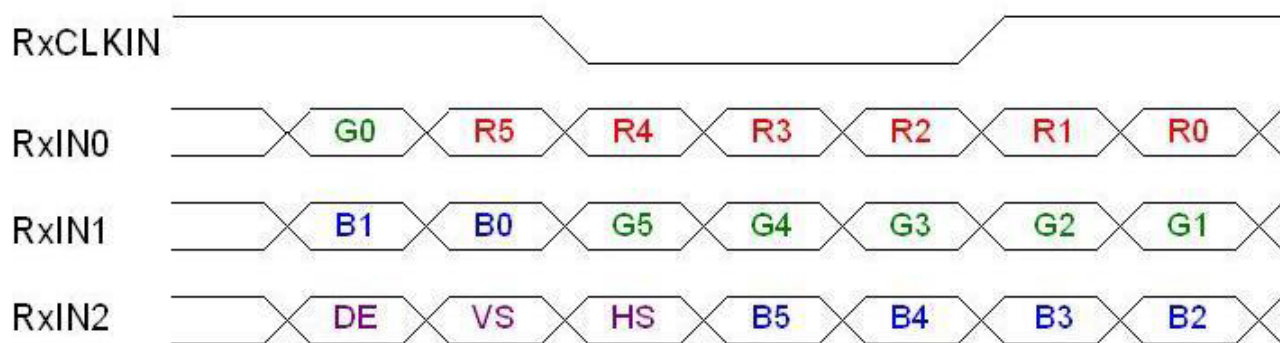
5.3 Signal Description

The module uses a LVDS receiver embedded in AUO's ASIC. LVDS is a differential signal technology for LCD interface and high-speed data transfer device.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DE)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be in low status when VDD is off.

Internal circuit of LVDS inputs are as following.



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data.
DE	Display Timing	When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	Vertical synchronized signal
HS	Horizontal Sync	Horizontal synchronized signal

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

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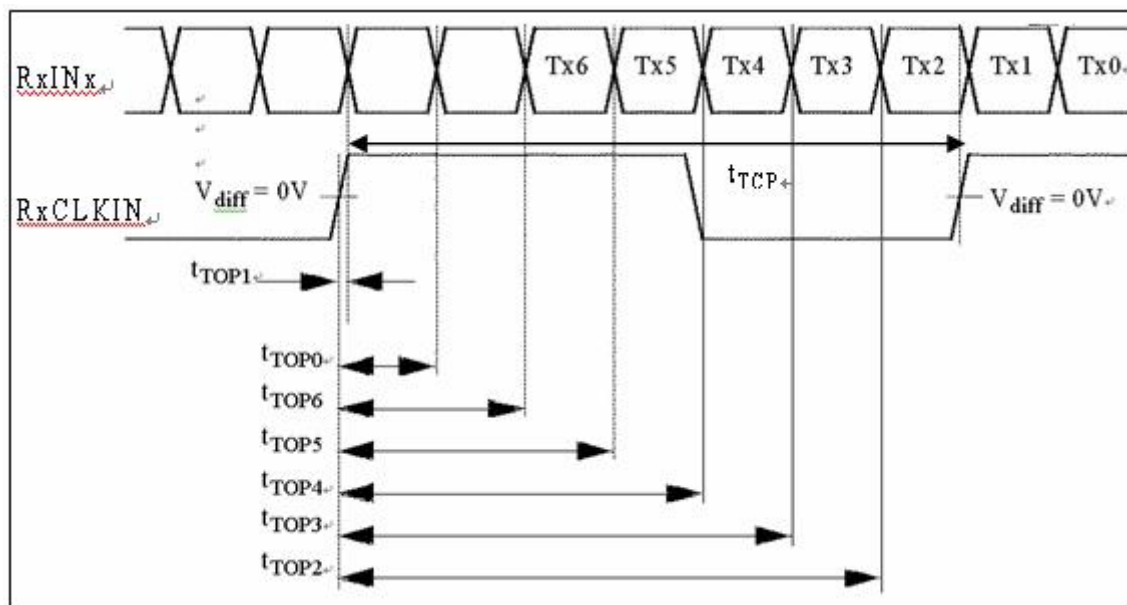
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5.4 Interface Timing



Note1. $RxINx$ can be $RxIN0, RxIN1$, or $RxIN2$.

Note2. $RxCLKIN$: Refer to the Signal Description in page 11 of this spec sheet.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCP}	CLK IN Period		T		
t_{TOP1}	Output Data Position1	-0.3	0	0.3	ns
t_{TOP0}	Output Data Position0	$T/7-0.3$	$T/7$	$T/7+0.3$	ns
t_{TOP6}	Output Data Position6	$2/7 T-0.3$	$2/7 T$	$2/7 T+0.3$	ns
t_{TOP5}	Output Data Position5	$3/7 T-0.3$	$3/7 T$	$3/7 T+0.3$	ns
t_{TOP4}	Output Data Position4	$4/7 T-0.3$	$4/7 T$	$4/7 T+0.3$	ns
t_{TOP3}	Output Data Position3	$5/7 T-0.3$	$5/7 T$	$5/7 T+0.3$	ns
t_{TOP2}	Output Data Position2	$6/7 T-0.3$	$6/7 T$	$6/7 T+0.3$	ns

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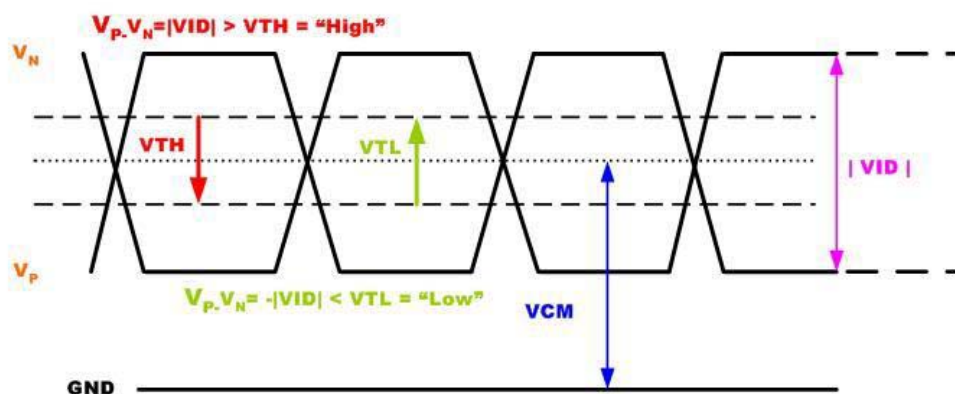
5.5 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off. It is recommended to refer the specifications.

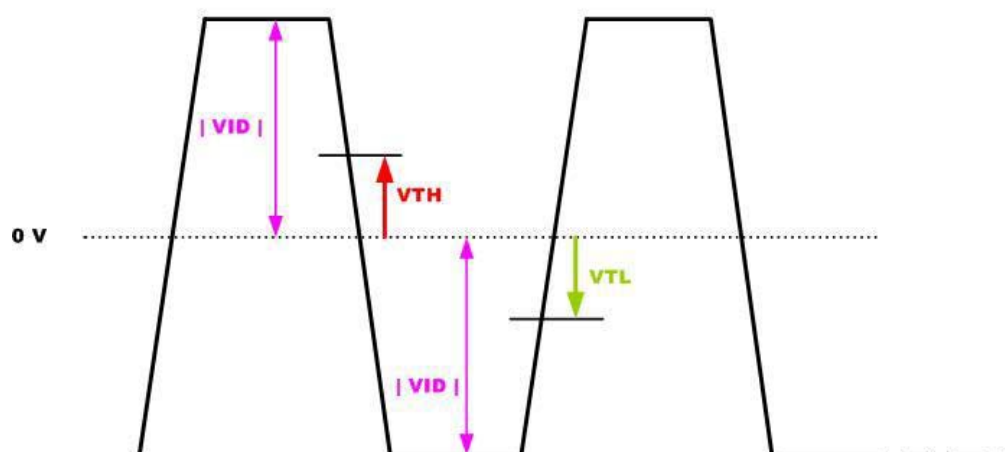
Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input voltage	VID	0.1	-	0.6	V	
LVDS input common mode voltage	VCM	1	1.2	1.5	V	VTH/VTL=+-100mV
Differential Input High Threshold Voltage	VTH	-	-	100	mV	VCM=1.2V
Differential Input Low Threshold Voltage	VTL	-100	-	-	mV	

Note: LVDS Signal Waveform

Single-end Signal



Differential Signal



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5.6 Signal for Lamp connector

Pin #	Signal Name
1	Lamp(A) High Voltage
2	Lamp(A) Low Voltage
3	Lamp(B) Low Voltage
4	Lamp(B) High Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0						1						1278						1279					
1st Line	R	G	B	R	G	B						R	G	B	R	G	B						
							
							
							
							
							
							
							
							
							
800th Line	R	G	B	R	G	B						R	G	B	R	G	B						



7.0 Parameter guide line for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
CCFL current(ICFL)	4.0	6.0	7.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(FCFL)	45	52	70	[KHz]	(Ta=25°C) Note 3
CCFL Starting Voltage (VSCFL)	1,200	—	—	[Volt] rms	(Ta= 0°C) Note 4 ; Note 6
CCFL Starting Voltage (VSCFL)	900	—	—	[Volt] rms	(Ta= 25°C) Note 4 ; Note 6
CCFL Voltage (Reference) (VCFL)	—	538	—	[Volt] rms	(Ta=25°C ICFL=6mA) Note 5
Single CCFL Power consumption (PCFL)	—	3.3	—	[Watt]	(Ta=25°C ICFL=6mA) Note 5

Note 1: Typ is AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying start-up voltage. It is recommended to keep on applying start-up voltage for 1 [Sec] until discharge.

*5 The CCFL inverter operating frequency must be carefully chosen so that no interfering noise stripes on the screen were induced.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter, which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: The CCFL inverter operating frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The inverter open voltage should be designed larger than the lamp starting voltage at T=0°C, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage. for longer than 1 second even if lamp connector is open.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

Note 6: CCFL Starting Voltage is defined the minimum starting voltage for inverter design reference.

8.0 Timing Control

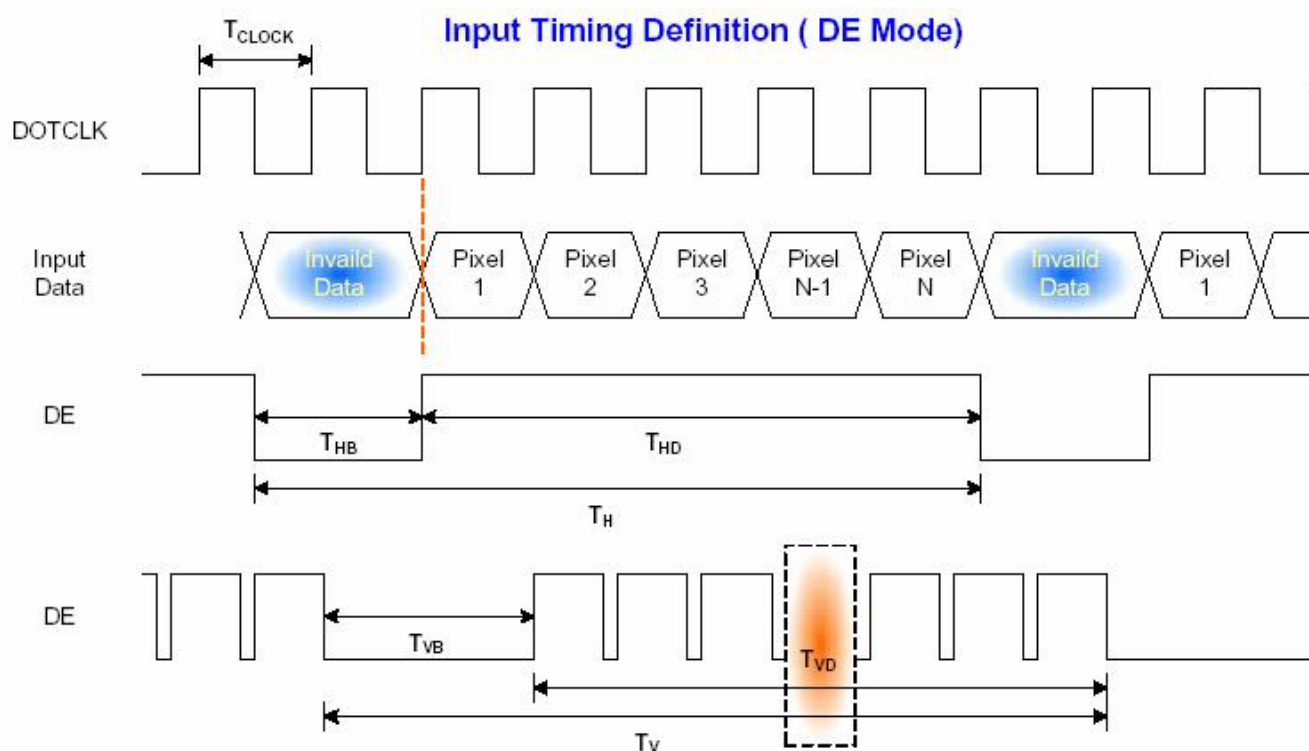
8.1 Timing Characteristics

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	62	68.9	75	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	

Note : DE mode only

8.2 Timing Definition



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9.0 Power Consumption

Input power specifications are as follows:

Symbol	Parameter	Min	Typ	Max	Units	Condition
Module						
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.6		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.7	[Watt]	Max Pattern (Note 1)
IDD	IDD Current		400		mA	64 Grayscale Pattern
IDD Max	IDD Current max			650	mA	Vertical stripe line Pattern (Note 1)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			500	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1: VDD=3.3V

Note 2: A121EW02 V0 Module includes four lamps.

Note 3: CCFL Starting Voltage is defined the minimum starting voltage for inverter design reference.

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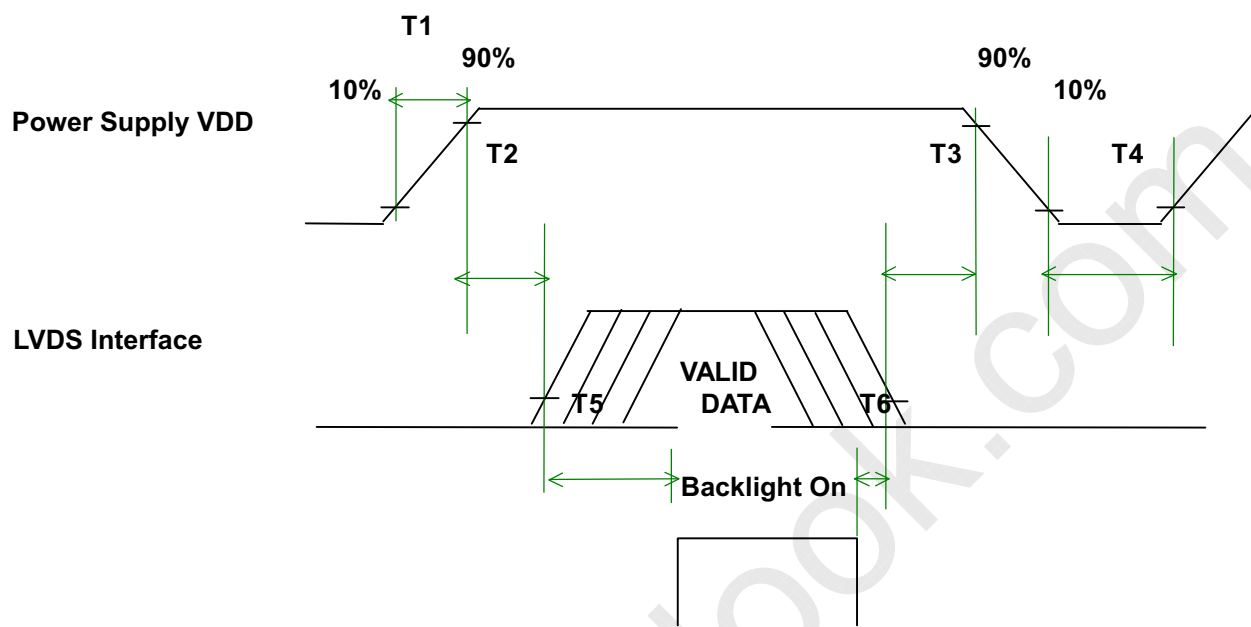
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10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.4	-	50	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	500	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)

Note 1: T5, T6 is only for assuring the display quality. (T5,T6 spec may be ignored if don't care the display quality.)

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11.0 Reliability /Safety Requirement

Reliability Test Conditions

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -20℃ 240Hrs	
3	High temperature operation	Tp= 71℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Tp= 50℃, 80% RH 240Hrs	Operation
6	Thermal shock	-20℃ to +60℃, Ramp ≤20℃/min, Duration at Temp. = 30min, Test Cycles = 50	Non-operation
7	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 3.0G, 33.3 ~ 400Hz Cycle : 15 minutes 2 hours for each direction of X,Z 4 hours for Y direction	JIS D1601, A-10 Condition A
8	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C0041, A-7 Condition C
9	Vibration (with carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/octave from 200~500Hz	IEC 68-34
10	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202
11	Electro Static discharge (ESD)	Contact Discharge: ±8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point. Air Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	Operation & Non-operation

Note1: Ta: Ambient temperature.

Note2: Tp: Center point temperature of Panel Surface.

Note3: All the cosmetic specification is judged before the reliability stress.

CCFL Life Time: 10,000 hours minimum

The" CCFL Life Time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃, I_L=6mA.

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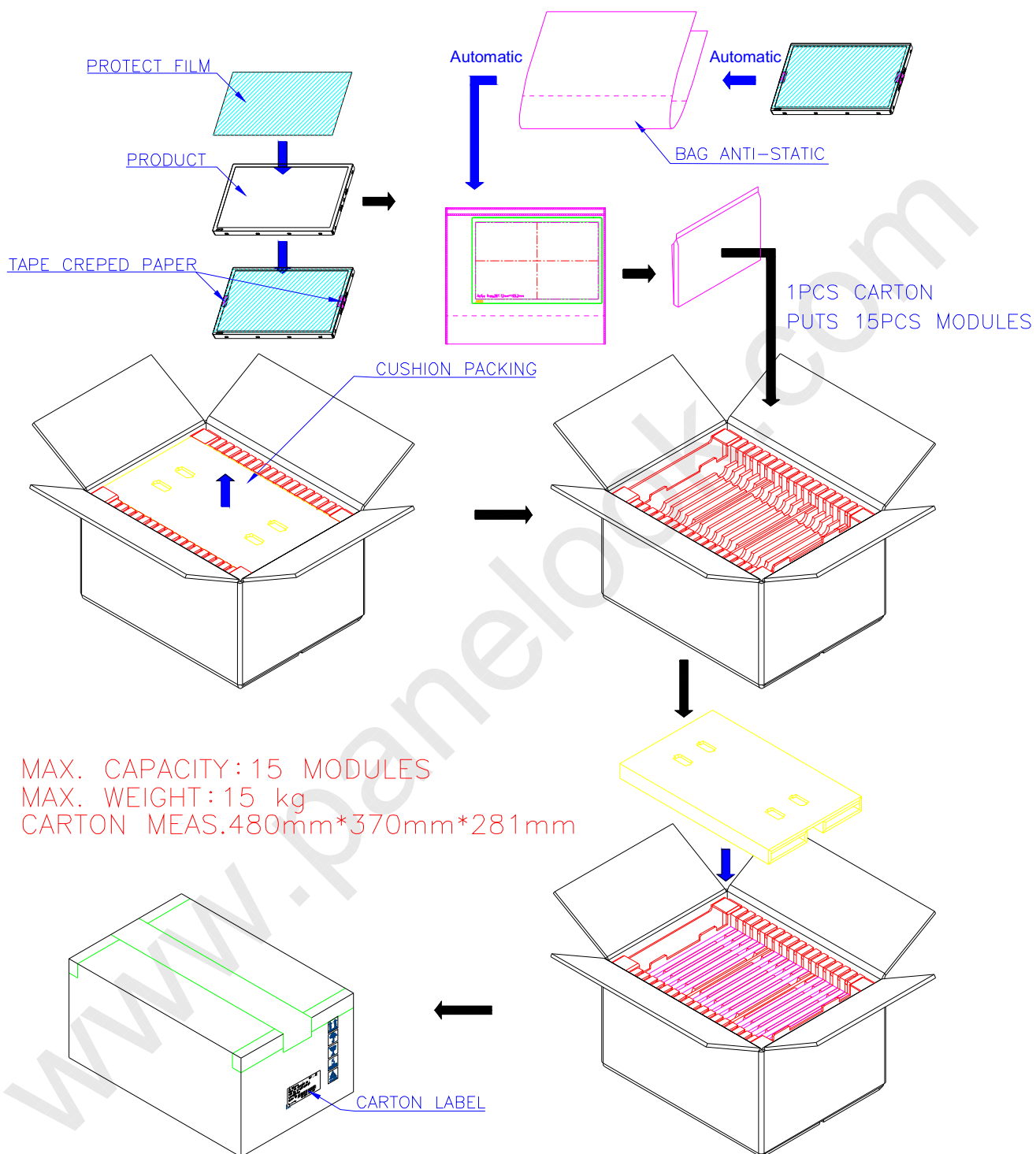
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14. Packaging description

A. Internal packaging



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B. External packaging

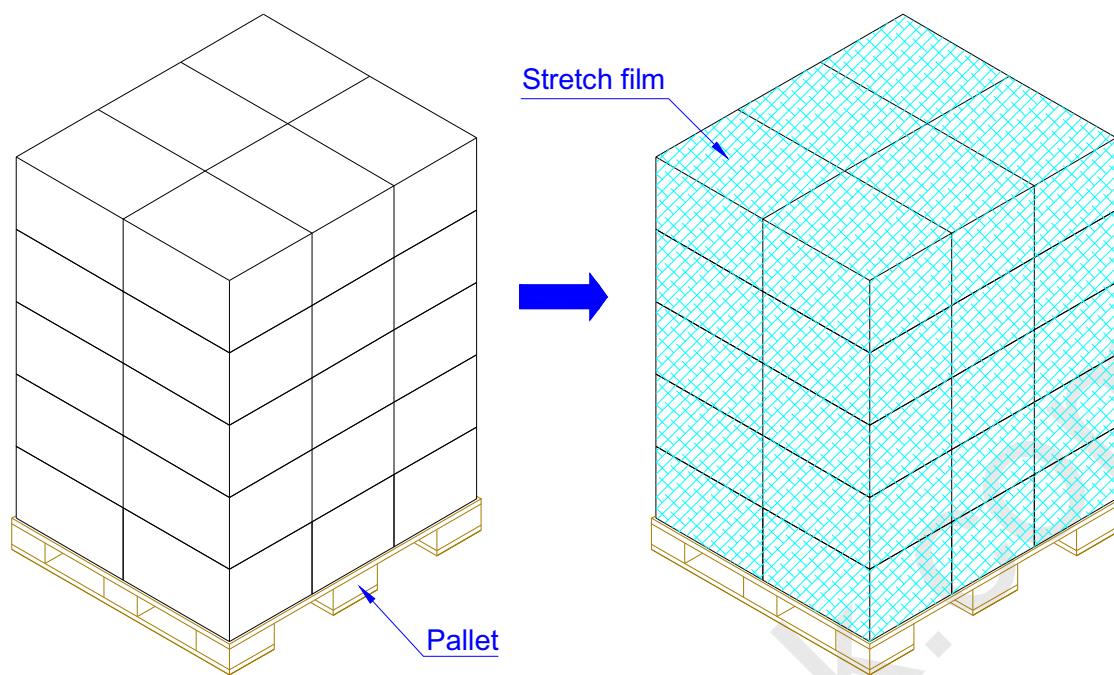
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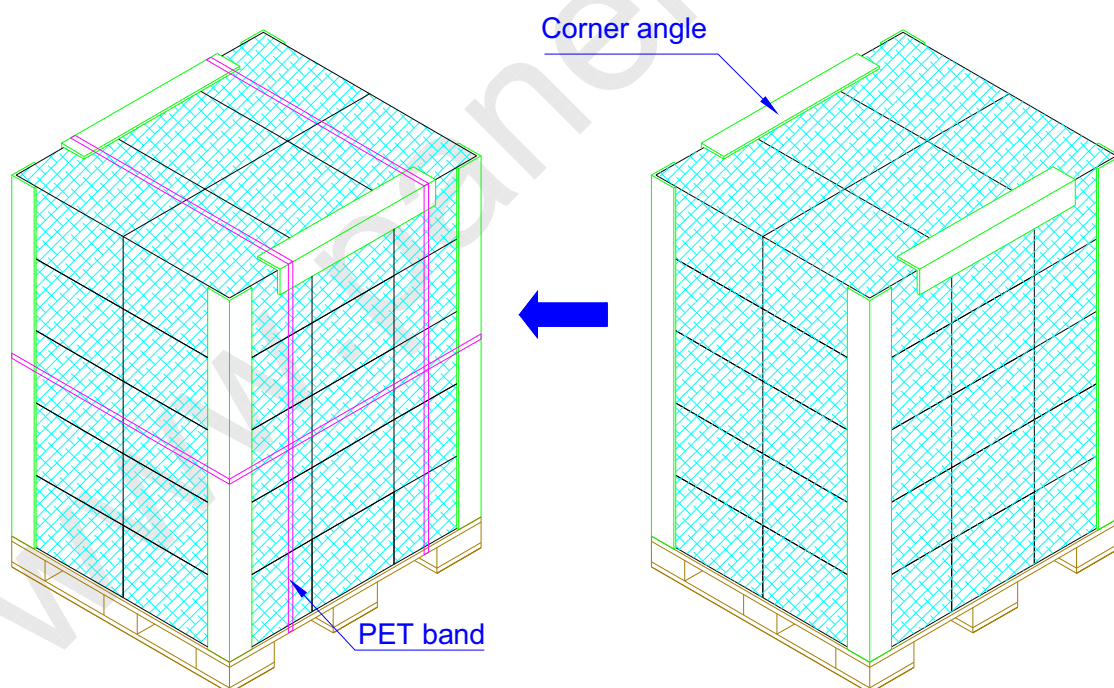
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Pallet: 1140mm*980mm

One pallet put 30 boxes(6boxes*5layers)



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